IN THE SPECIFICATION:

Please amend paragraph number **[0039]** as follows:

[0039] After channels 16 have been cut and etched, FIG. 5 shows that a protective coating 42 is formed on wafer 2 to cover active surface 8 and fill channels 16. Protective coating 42 may comprise a liquid polymer sealant material that is sprayed, spin coated or otherwise dispensed onto wafer 2 and then hardened by thermal or ambient temperature curing. One liquid polymer sealant material suitable for protective coating 42 is commercially available from 3D Systems, Inc. of Valencia, CA, under the product name ~~Acura~~ Accura® SI 40. FIG. 5 shows that protective coating 42 is formed with apertures 44 exposing bond pads 14 in order to allow subsequent electrical connection. In order to form apertures 44, the entire active surface 8 of wafer 2 may be covered, with apertures 44 being formed by subsequent removal of portions of protective coating 42, such as by masking and etching protective coating 42.

Please amend paragraph number **[0044]** as follows:

[0044] Turning to FIG. 7, in this alternative, after protective coating 42 is formed on active surface 8, wafer 2 is subjected to a backgrinding or other planarization process prior to being completely separated. This removes excess semiconductor material from passive surface 12 of wafer 2 to reduce the thickness of wafer 2 to a desired overall thickness. Several types of processes are available to perform the thinning of the wafer 2. Either a mechanical grinding process or an abrasive planarization process such as chemical-mechanical planarization (CMP) may be used to remove material from passive surface 12 of wafer 2. For example, in FIG. 7, a grinding wheel 60 may be applied to passive or ~~backside~~ back side surface 12 of wafer 2 to abrade material therefrom. Alternatively, passive surface 12 of wafer 2 may be chemically etched to remove material. The particular mechanism for thinning wafer 2 is considered to be a matter of convenience to those of ordinary skill in the semiconductor process manufacturing area. As seen in FIG. 7, semiconductor material is removed from passive surface 12 to a depth sufficient to expose protective coating 42 contained in channels 16.